CLAIMS:

1. Circuit (1) for driving a display panel (3) that comprises a matrix of pixels (P_{ij}), the matrix comprising a plurality of rows (i) and columns (j), the circuit comprising:

- an input for receiving an input signal (V_1) comprising pixel values (s_{ij}) for the plurality of rows (i) in a frame to be displayed by at least some of the pixel (P_{ij}), each pixel value (s_{ij}) determining a light output of a pixel (P_{ij});
- a memory (9) for storing the received pixel values (s_{ij});
- processing circuitry (10) for analyzing the pixel values (s_{ij}) in each of the plurality of rows (i) and for generating a row timing signal ($Hsync_2$) for addressing a subset of the plurality of rows (i) for substantially a duration of a row time ($t_{row2}(i)$) being a time period for addressing a row, and
- a video output for supplying an output signal (V_2) comprising output pixel values to pixels (P_{ij}) in the subset of rows (i) being addressed,

wherein the processing circuitry (10) is arranged to determine each row time ($t_{row2}(i)$) in dependence on at least one pixel value (s_{ij}) from among the pixel values (s_{ij}) for the subset of rows (i) being addressed during that row time ($t_{row2}(i)$).

2. Circuit (1) according to claim 1, wherein the circuitry (10) is arranged to determine the row times ($t_{row2}(i)$) such that all of the subsets of rows (i) in a frame are addressed within a frame time (t_f), being a time period for addressing the plurality of rows (i) in the frame, and that the frame time (t_f) remains substantially constant over a number of consecutive frames.

3. Circuit (1) according to claim 1, wherein the circuitry (10) is arranged to determine the value of each row time ($t_{row2}(i)$) in dependence on a maximum value (h_i) from among the pixel values (s_{ij}) for the subset of rows being addressed during that row time $t_{row2}(i)$).

4. Circuit (1) according to claim 3, wherein the circuitry (10) is arranged to supply via the video output the output pixel values in the form of a pulse-width modulated signal.

5. Circuit (1) according to claim 4, the processing circuitry (10) comprising a sub-circuit for generating a clock signal (pix_clk_2) having a clock period, each pulse width in the pulse-width modulated signal being a number of the clock periods, wherein the circuitry (10) is arranged to determine the clock period for each frame by dividing the frame time (t_f) by a sum (S) of the maximum pixel values (h_i).

6. Circuit (1) according to claim 4, the circuitry (10) comprising a sub-circuit (10) for generating a clock signal (pix_clk_2) having a clock period, each pulse width in the pulse-width modulated signal being a number of the clock periods, and a look-up table of possible clock periods, wherein the circuitry (10) is arranged to determine the sum (S) of the maximum pixel values (h_i), and to select the clock period from the look-up table on the basis of the sum (S) calculated.

7. Circuit (1) according to claim 4, wherein the circuitry (10) comprises a sub-circuit for generating a clock signal (pix_clk_2) having a clock period, each pulse width in the pulse width modulated signal being a number of the clock periods, wherein the circuitry (10) is arranged to set the clock period of a frame to a value determined by averaging clock periods determined for a number of consecutive frames.

8. Circuit (1) according to claim 1, arranged to generate via the video output the output signal (V_2) corresponding to an amplitude of a signal to be supplied to a pixel (P_{ij}).

9. Display device, comprising a display panel (3) that comprises a matrix of pixels (P_{ij}), which matrix comprises a plurality of rows (i) and at least one column (j), wherein the circuit (1) according to claim 1 is present.

10. Method of driving a display panel (3) that comprises a matrix of pixels (P_{ij}), which matrix comprises a plurality of rows (i) and columns (j), the method comprising the steps of:

receiving an input signal (V_1) comprising pixel values (s_{ij}) for the plurality of

rows (i) in a frame to be displayed by at least some of the pixels (P_{ij}), each pixel value (s_{ij}) determining a light output of a pixel (P_{ij});

- storing the received pixel values (s_{ij}) in a memory (9),
- analyzing the pixel values (s_{ij}) in each of the plurality of rows (i);
- generating a row timing signal ($Hsync_2$) for addressing a subset of the plurality of rows (i) for substantially a duration of a row time ($t_{row2}(i)$) being a time period for addressing a row; and
- supplying an output signal (V_2) comprising output pixel values to pixels (P_{ij}) in the subset of rows (i) being addressed,

wherein, during analyzing the pixel value(s) (s_{ij}) in each of the plurality of rows (i), each row time ($t_{row2}(i)$) is determined in dependence on at least one pixel value from among the pixel values for the subset of rows being addressed during that row time ($t_{row2}(i)$).